IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		TI-36593
	Jaroslav Hynecek	Art Unit: 2622
Serial No:	10/683,966	Examiner: Tuan V. Ho
Filed:	October 10, 2003	Conf. No.: 1855

For: Low Noise Image Sensing System and Method for Use With Sensors With Very Small Pixel Size

Appeal Brief Under 37 C.F.R. §41.37

Board of Patent Appeals and Interferences
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to 37 C.F.R. §41.37 in connection with the above-identified application in response to the Final Rejection mailed October 22, 2007, and the Petition to Revive and Notice of Appeal mailed by Applicant on October 24, 2008.

Real Party in Interest

The real party in interest in this application is Texas Instruments Incorporated, a corporation of Delaware with its principle place of business in Dallas, Texas. An assignment to Texas Instruments Incorporated is recorded at reel 013275 and frame 0196 to 0198.

Related Appeals and Interferences

There are no appeals of interferences related to this appeal in this application.

Status of the Claims

Claims 1-13 are the subject of this appeal. Claims 1-13 are rejected. This application was filed on October 10, 2003.

Status of Amendments Filed After Final Rejection

The Appellants filed an amendment under 37 C.F.R. § 1.116 on December 12, 2007 in response to the Office Action dated October 22, 2007, with no amendments to the claims.

Summary of Claimed Subject Matter

Claim 1:

Specification page 6, line 11 to page 7, line 13, provides a concise explanation of the invention defined in claim 1.

In the imaging system of FIG. 2, signal charge is only partially integrated in the sensor pixels due to their small size and is quickly read out several times during one frame time cycle. The signal integration is completed in the digital domain after the analog output is converted to a digital form. The signal integration after readout has many advantages in reducing photon noise; kTC reset noise, and digitization noise as well as in increasing the sensor dynamic range independently of pixel size.

Image sensing area 201, pixels 202, and all the components from 203 to 217 correspond to the same system components from 101 to 117 of drawing 100 shown in FIG. 1. The difference between the conventional and the new system is only in the sensor readout speed, number of readouts in one frame time cycle and in processing the digitized signal. The digital signal received from A/D converter 206 is loaded into digital shift register 218. When a complete line of data is loaded into the register the same line of data from previous scans is fetched from memory 220 and placed into line adder 219. In the subsequent step, the data from register 218 is summed with the data brought back from the memory and the result is placed back into the memory. These steps accomplish the digital pixel integration and memory locations 213 now store the integrated pixel signal. The signal can be read from memory 220 after completion of frame integration time cycle by supplying addressing data through lines 216 and 217 to memory addressing registers 214 and 215. The data appears on digital buses 209 and 210 and after conversion to analog form by D/A converter 211 is available for analog display on line 212.

Claim 5:

Specification page 6, line 11 to page 7, line 13, provides a concise explanation of the invention defined in claim 5.

In the imaging system of FIG. 2, signal charge is only partially integrated in the sensor pixels due to their small size and is quickly read out several times during one frame time cycle. The signal integration is completed in the digital domain after the analog output is converted to a digital form. The signal integration after readout has many advantages in reducing photon noise; kTC reset noise, and digitization noise as well as in increasing the sensor dynamic range independently of pixel size.

Image sensing area 201, pixels 202, and all the components from 203 to 217 correspond to the same system components from 101 to 117 of drawing 100 shown in FIG. 1. The difference between the conventional and the new system is only in the sensor readout speed, number of readouts in one frame time cycle and in processing the digitized signal. The digital signal received from A/D converter 206 is loaded into digital shift register 218. When a complete line of data is loaded into the register the same line of data from previous scans is fetched from memory 220 and placed into line adder 219. In the subsequent step, the data from register 218 is summed with the data brought back from the memory and the result is placed back into the memory. These steps accomplish the digital pixel integration and memory locations 213 now store the integrated pixel signal. The signal can be read from memory 220 after completion of frame integration time cycle by supplying addressing data through lines 216 and 217 to memory addressing registers 214 and 215. The data appears on digital buses 209 and 210 and after conversion to analog form by D/A converter 211 is available for analog display on line 212.

Claim 10:

Specification page 6, line 11 to page 7, line 13, provides a concise explanation of the invention defined in claim 10.

In the imaging system of FIG. 2, signal charge is only partially integrated in the sensor pixels due to their small size and is quickly read out several times during one frame time cycle. The signal integration is completed in the digital domain after the analog output is converted to a digital form. The signal integration after readout has many advantages in reducing photon noise; kTC reset noise, and digitization noise as well as in increasing the sensor dynamic range independently of pixel size.

Image sensing area 201, pixels 202, and all the components from 203 to 217 correspond to the same system components from 101 to 117 of drawing 100 shown in FIG. 1. The difference between the conventional and the new system is only in the sensor readout speed, number of readouts in one frame time cycle and in processing the digitized signal. The digital signal received from A/D converter 206 is loaded into digital shift register 218. When a complete line of data is loaded into the register the same line of data from previous scans is fetched from memory 220 and placed into line adder 219. In the subsequent step, the data from register 218 is summed with the data brought back from the memory and the result is placed back into the memory. These steps accomplish the digital pixel integration and memory locations 213 now store the integrated pixel signal. The signal can be read from memory 220 after completion of frame integration time cycle by supplying addressing data through lines 216 and 217 to memory addressing registers 214 and 215. The data appears on digital buses 209 and 210 and after conversion to analog form by D/A converter 211 is available for analog display on line 212.

Grounds for Rejection to be Reviewed on Appeal

Whether claims 1-3, 5, 6, 8, 10, 12, and 13 are unpatentable under 35 USC 102(b) over U.S. Patent No. 5,365,269.

Whether claims 4, 9, and 11 are unpatentable under 35 USC 103(a) over U.S. Patent No. 5,365,269 and U.S. Patent No. 5,630,064.

Whether claim 7 is unpatentable under 35 USC 103(a) over U.S. Patent No. 5,365,269 and Applicant's Admitted Prior Art.

Arguments

Rejection under 35 USC 102(b) as being unpatentable over U.S. Patent No. 5,365,269

Claims 1-3, 5, 6, 8, 10, 12, and 13

Claim 1 includes "... repeating the above steps N times during a frame time cycle ...". Claim 5 includes "…repeating the above steps N times during a frame time cycle, … and performing digital integration in the digital memory device by cumulatively combining the digital signal of a present step with the digital signal of previous steps." Claim 10 includes "… wherein the digital memory device cumulatively combines an output from each pixel with an output from a previous readout of each pixel each time the array of image sensing pixels is readout during a frame time cycle." The references of record do not show, teach, or suggest the above recited limitations of claims 1, 5, and 10. U.S. Patent No. 5,365,269 does not teach repeating the charge integration steps multiple times in a frame time. U.S. Patent No. 5,365,269 teaches taking the charge integration from multiple frames and combining the data by shifting the pixel data to match up with the location of the object in the first step, then combining the data. See column 5, lines 41-42. U.S. Patent No. 5,365,269 is clearly combining data from multiple frames, not from multiple readouts during a single frame time, because the data has to be shifted to fit the new frame to the previous frame after each charge integration step.

Rejection under 35 USC 103(a) as being unpatentable over U.S. Patent No. 5,365,269 and U.S. Patent No. 5,630,064

Claims 4, 9, and 11

Claim 4 depends from claim 1. Claim 1 includes "... repeating the above steps N times during a frame time cycle ...". Claim 9 depends from claim 5. Claim 5 includes "…repeating the above steps N times during a frame time cycle, … and performing digital integration in the digital memory device by cumulatively combining the digital signal of a present step with the digital signal of previous steps." Claim 11 depends from claim 10. Claim 10 includes "… wherein the digital memory device cumulatively combines an output from each pixel with an output from a previous readout of each pixel each time the array of image sensing pixels is readout during a frame time cycle." The references of record do not show, teach, or suggest the above recited limitations of claims 1, 5, and 10. U.S. Patent No. 5,365,269 does not teach repeating the charge integration steps multiple times in a frame time. U.S. Patent No. 5,365,269 teaches taking the charge integration from multiple frames and combining the data by shifting the pixel data to match up with the location of the object in the first step, then combining the data. See column 5, lines 41-42. U.S. Patent No. 5,365,269 is clearly combining data from multiple frames, not from multiple readouts during a single frame time, because the data has to be shifted to fit the new frame to the previous frame after each charge integration step. Therefore, U.S. Patent No. 5,365,269 and U.S. Patent No. 5,630,064 combined do not teach the limitations of claims 4, 9, and 11.

Rejection under 35 USC 103(a) as being unpatentable over U.S. Patent No. 5,365,269 and Applicant's Admitted Prior Art

Claim 7

Claim 7 depends from claim 5. Claim 5 includes "...repeating the above steps N times during a frame time cycle, ... and performing digital integration in the digital memory device by cumulatively combining the digital signal of a present step with the digital signal of previous steps." The references of record do not show, teach, or suggest the above recited limitations of claims 5. U.S. Patent No. 5,365,269 does not teach repeating the charge integration steps multiple times in a frame time. U.S. Patent No. 5,365,269 teaches taking the charge integration from multiple frames and combining the data by shifting the pixel data to match up with the location of the object in the first step, then combining the data. See column 5, lines 41-42. U.S. Patent No. 5,365,269 is clearly combining data from multiple frames, not from multiple readouts during a single frame time, because the data has to be shifted to fit the new frame to the previous frame after each charge integration step. Therefore U.S. Patent No. 5,365,269 and Applicant's Admitted Prior Art combined do not teach the limitations of claim 7.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-13 is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

To the extent necessary, the Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 20-0668 of Texas Instruments Inc.

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,

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CLAIMS APPENDIX

1. A method for sensing an image comprising:

integrating charge in an image sensor array;

transferring the charge out of the image sensor array;

converting the charge to a digital signal;

combining the digital signal with digital data stored in a memory device to form an integrated signal;

storing the integrated signal in the memory device such that the integrated signal becomes the digital data; and

repeating the above steps N times during a frame time cycle, where N is an integer greater than one.

2. The method of claim 1 wherein the step of the combining the digital signal with the digital data comprises summing the digital signal and the digital data to form the integrated signal.

3. The method of claim 1 wherein the step of storing the integrated signal comprises storing the integrated signal in addresses corresponding to pixels in the image sensor array.

4. The method of claim 1 wherein the step of combining the digital signal with the digital data comprises:

loading a line of data from the digital signal into a digital shift register;

retrieving a data line of the digital data from a corresponding location in the memory device;

summing the line of data with the data line from the memory device; and

storing the integrated signal back into the corresponding location in the memory device.

5. A method for sensing an image comprising:

integrating charge in pixels of an image sensor array in response to incident light;

providing an analog output signal from the image sensor array that indicates charge levels for each pixel in the array;

converting the analog output signal to a digital signal;

transferring the digital signal to a digital memory device;

repeating the above steps N times during a frame time cycle, where N is an integer greater than one; and

performing digital integration in the digital memory device by cumulatively combining the digital signal of a present step with the digital signal of previous steps.

6. The method of claim 5 further comprising reading a digital image signal from the memory device.

7. The method of claim 6 further comprising converting the digital image signal to an analog signal.

8. The method of claim 5 further comprising storing the digital signal in addresses corresponding to each pixel in the image sensor array.

9. The method of claim 5 wherein the step of performing digital integration comprises:

loading a line of data from the digital signal into a digital shift register;

retrieving a data line from a corresponding location in the memory device;

summing the line of data with the data line from the memory device to form an integrated signal; and

storing the integrated signal back into the corresponding location in the memory device.

10. An image sensing device comprising:

an array of image sensing pixels;

an analog-to-digital converter coupled to an output of the array;

a digital memory device coupled to an output of the converter, wherein the digital memory device cumulatively combines an output from each pixel with an output from a previous readout of each pixel each time the array of image sensing pixels is readout during a frame time cycle.

11. The device of claim 10 wherein the digital memory device comprises:
a digital shift register coupled to the output of the analog-to-digital converter;
an adder coupled to the digital shift register; and
a digital memory array coupled to the adder.

12. The device of claim 10 further comprising a shift register coupled to the array of image sensing pixels.

13. The device of claim 12 further comprising a buffer amplifier coupled between the shift register and the analog-to-digital converter.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None